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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,006	12/29/2000	Joseph A. Bennett	42390.P9942	9847

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EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/30/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,006	BENNETT, JOSEPH A.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the RCE filed on 07/07/04 in application 09/753,006.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-13, and 15-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable Egan et al. (US Patent 5,875,308 hereafter referred to as Egan) in view of Zhang et al. (U.S. Patent 6,457,082 hereafter referred to as Zhang).

As per claim 1:

Egan substantially teach the invention. Egan teaches:

- a system comprising:

- a bus including power line [col. 2, lines 17-27];

- a bus bridge device including an internal logic unit [col. 3, lines 1-11 and lines 47-60];

- a power regulator to delivery power to the power lines [col. 3, lines 66 through col. 4, lines 17 and col. 4, lines 60 through col. 5, lines 2];

- the power regulator [col. 3, lines 66 through col. 4, lines 17 and col. 4, lines 60 through col. 5, lines 2] to assert a fault signal to the bus bridge device if a power fault is detected [col. 3, lines 59].

Egan does not explicitly teach:

- a bus bridge device to disconnect the internal logic unit from the bus in response to an assertion of the fault signal.

However, Egan does disclose capability of:

- Peripheral component interconnect (PCI) architecture having hot-plugging capability for a data processing system [abstract, fig. 1, col. 1, lines 9-15] comprising:

- PCI hot-plug bridge 21 having I/O pins namely, power-on reset, load clock, shift clock, data in, data out functions (i.e., internal logic unit) [col. 3, lines 47];
- power failure detection [fig. 1 and 2, col. 5, lines 23-34]].

In addition, Zhang explicitly teaches:

- A break event generation during transition between modes of operation in a computer system [abstract, fig. 1, col. 1, lines 17-24] comprising:
- ***A bus bridge device*** used within computer system to detect and break event in response to failure [col. 3, lines 10-22 and col. 5, lines 27-54].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Egan's PCI hot-plug bridge 21 having I/O pins namely, power-on reset, load clock, shift clock, data in, data out functions (i.e., internal logic unit) used to support- power failure detection as being as claimed by Applicant. This is because Egan does perform data failure detection, monitoring, and correction via the PCI hot plug bridge 21 [col. 4, lines 39-53] as well as depicted in figures 1 and 2 in ensuring computer

system functioned properly; second, by applying ***A bus bridge device*** used within computer system to detect and break event in response to failure as taught by Zhang's break event generation during transition between modes of operation in a computer system in conjunction with the Egan's Peripheral component interconnect (PCI) architecture having hot-plugging capability for a data processing system in order to enhance the computer system bus performance, more specifically to ensuring the system error detected, corrected, and replaced in proper and efficient manner. One of ordinary skill in the art would have been motivated to do so to improve the system bus access, data transmission availability and integrity.

As per claims 3-5:

Egan further teaches:

- a power regulator to cease to deliver power to the power line if a power fault is detected [col. 3, lines 66 through col. 4, lines 17 and col. 4, lines 60 through col. 5, lines 2];

- a bus bridge device to assert an interrupt signal in response to the assertion of the fault signal[col. 4, lines 18-37];

- the bus bridge device to assert an error signal in response to the assertion of the fault signal (i.e., bus bridge power monitoring input/notification) [col. 4, lines 38-53].

In addition, Zhang further teaches:

- ***A bus bridge device*** used within computer system to detect and break event in response to failure [col. 3, lines 10-22 and col. 5, lines 27-54];

- power detection and disconnection [col. 16, lines 53-56].

As per claims 6-9:

Egan further teaches:

- a bus bridge device to assert a power enable (i.e., turn power on) signal to the power regulator [col. 3, lines 66 through col. 4, lines 17 and col. 4, lines 60 through col. 5, lines 2] upon system startup [col. 4, lines 2-17];

- the bus bridge deassert the power enable signal follow the assertion of the fault signal [col. 3, lines 66 through col. 4, lines 53];

- a power regulator module to deassert the fault signal in response to the deassertion of the power enable signal [col. 3, lines 66 through col. 4, lines 59];

- the bus is a PCI bus [col. 2, lines 59-63].

In addition, Zhang further teaches:

- ***A bus bridge device*** includes a plurality of programmable registers that are used to configure the break event (i.e., disable resources) [col. 16, lines 29-31 and lines 46-48];
- power detection and disconnection [col. 16, lines 53-56].

As per claims 10-12:

These claims are the same as per claims 1, 3-9. The only minor different is that these claims are directed to **a bus bridge device** instead of the system comprising a bus bridge device as described in claims 1-9. However, Egan's enhanced peripheral component interconnect (PCI) architecture for a data processing explicitly teaches a bus bridge device [col. 3, lines 1-11 and lines 47-60]. Therefore, these claims are also rejected under the same rationale applied against claims 1, 3-9.

As per claims 13, 15-16:

Due to the similarity of claims 13, 15-16 to claims 1, 3-9 except for a method comprising applying power step, detecting power step, asserting a fault signal step, etc… instead a system comprising capabilities of detecting power, deliver power,

asserting fault signal, etc...therefore, these claims are also rejected under the same rationale applied against claims 1, 3-9. **In addition, all of the limitations have been noted in the rejection as per claims 1, 3-9.**

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
11/23/04